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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/721,097 | 11/26/2003 | Masanori Matsuura | 60188-720 | 6177 |

7590 06/30/2006

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| EXAMINER | |
|---|---|
| KIM, DANIEL Y | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2185 | |

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/721,097 | MATSUURA, MASANORI | |
| | Examiner | Art Unit | |
| | Daniel Kim | 2185 | |

*– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 April 2006 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to applicant's communication filed April 20, 2006 in response to the PTO Office Action mailed January 17, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1 and 11 have been amended, and no other claims have been canceled or added. Claims 1-12 remain pending in this application.

### *Response to Arguments*

3. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al (US Patent No. 6,400,625) and Shiga et al (US Patent No. 6,552,936).

Arimoto discloses a storage device, comprising:

a memory (a system LSI equipped with a memory, col. 1, lines 12-13);

a microcomputer for taking in data read from the memory according to a externally-supplied clock signal or a clock signal generated based on the externally-supplied clock signal (a system LSI such as a logic merged DRAM in which a logic such as a processor and an application specific integrated circuit and a dynamic random access memory of mass storage capacity are integrated on one semiconductor chip, col. 1, lines 17-21);

a timing signal output circuit for outputting a timing signal indicative of a timing that is shifted by a predetermined time period, which is determined according to a frequency of the clock signal, from a predetermined edge in a read control signal which is used for controlling reading of data from the memory (multiplying the frequency of an external test clock signal, which is input from an external memory tester, for example, to an internal test clock signal having a different frequency, a data shifter shifting test output data transmitted from a read data selection circuit for a period corresponding to a timing control signal generated, col. 7, lines 46-53); and

a read data control circuit for performing control such that the microcomputer takes in the data read from the memory (col. 7, lines 46-53).

Arimoto fails to disclose the remaining claim limitations.

Shiga, however, helps disclose a read data control circuit for performing control such that the microcomputer takes in the data read from the memory based on the timing signal only when the clock signal has a predetermined frequency between an upper limit and a lower limit determined according to the shift of the timing (an upper limit and lower limit of the frequency of an external clock is determined by a values which can continuously be outputted without delay, col. 9, lines 15-28).

Arimoto and Shiga are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include upper and lower limits to a frequency because an external clock frequency fluctuates with a system in which the chip is mounted, and is not constant, and limits can continuously be outputted without delay in pipeline operation (col. 9, lines 21-25), as taught by Shiga.

Claim 2 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 3, the combined teachings of Arimoto and Shiga disclose the invention as per rejection of claim 2 above.

Arimoto further helps disclose the read data control circuit controls whether or not the data read from the memory is output to the microcomputer based on the relationship between the timing which is indicated by the timing signal and the timing at which an edge subsequent to the predetermined edges occurs in the read control signal (valid read data is output at a rising edge of a test clock signal in a clock cycle according to internal read command applied to a different clock cycle, col. 4, lines 29-31; read data

selection circuit outputs read data in a clock cycle which corresponds to the rising edge of the external test clock signal in a separate clock cycle, therefore read data may be output as test output data, col. 11, lines 66-67, col. 12, lines 1-3).

Claim 5 is rejected using the same rationale as for the rejection of claim 2 above.

6. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al (US Patent No. 6,400,625), Shiga et al (US Patent No. 6,552,936) and Hamamoto et al (US PGPub No. 20020141280).

For claim 4, the combined teachings of Arimoto and Shiga disclose the invention as per rejection of claim 3 above.

These teachings fail to disclose the limitations of the current claim.

Hamamoto, however, helps disclose when the read data control circuit does not output the data read from the memory to the microcomputer, the read data control circuit outputs data different from the data read from the memory (a reading circuit includes a preamplifier for amplifying data read from a memory circuit, and a latency shifter for shifting output data of preamplifier for a predetermined period of time, and that data may be transmitted to a data output circuit, or may be coupled to a contentional data output circuit responsive to an output control clock signal having a non-adjusted phase, par. 0247).

Arimoto, Shiga and Hamamoto are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to

include a read data control circuit outputting data different from data read from a memory because this would allow for output data with or without a latency shift (par. 0247), as taught by Hamamoto.

Claim 6 is rejected using the same rationale as for the rejections of claims 4 and 5 above.

7. Claims 7-8 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al (US Patent No. 6,400,625), Shiga et al (US Patent No. 6,552,936) and Sawada et al (US Patent No. 6,157,992).

For claim 7, the combined teachings of Arimoto and Shiga disclose the invention as per rejection of claim 2 above.

These teachings fail to disclose the limitations of the current claim.

Sawada, however, helps disclose a mask circuit for the outputting of the data read from the memory to the microcomputer for a predetermined time period, wherein the read data control circuit performs control such that the microcomputer takes in data output from the mask circuit at a predetermined timing that is determined according to the timing signal (a mask enable circuit delaying internal mask instruction signal for a predetermined period, and an output control circuit outputting an output enable signal enabling data output operation of an output buffer circuit according to data read enable signal from read enable circuit and mask enable signal from mask enable circuit, col. 2, lines 20-28).

Arimoto, Shiga and Sawada are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a mask enable circuit because this would allow for masking output data (col. 1, line 48) and delaying an internal mask instructing signal for a predetermined period (col. 2, lines 20-21), as taught by Sawada.

Claim 8 is rejected using the same rationale as for the rejections of claims 6 and 7 above.

Claim 11 is rejected using the same rationales as for the rejections of claims 1 and 7 above.

For claim 12, the combined teachings of Arimoto, Shiga and Sawada disclose the invention as per the rejection of claim 11 above.

Sawada further helps disclose the timing control circuit sets the predetermined time period during which the mask circuit outputs the data read from the memory and the timing for taking the data output from the mask circuit into the microcomputer is based on a predetermined signal output from the microcomputer (a read enable signal generating circuit generates a read enable signal activated for a predetermined time period in response to read operation triggering signal from a read command decoder, and an output control circuit receiving internal mask instructing signal from a buffer circuit and read enable signal to generate a data output enable signal for application to an output buffer circuit, col. 6, lines 46-53).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al (US Patent No. 6,400,625), Shiga et al (US Patent No. 6,552,936) and Chevallier (US Patent No. 6,002,627).

For claim 9, the combined teachings of Arimoto and Shiga disclose the invention as per the rejection of claim 1 above.

These teachings fail to disclose the limitations of the current claim.

Chevallier, however, helps disclose a temperature detection circuit, wherein the read data control circuit performs control such that the microcomputer takes in the data read from the memory only when the temperature detection circuit detects a predetermined temperature (an integrated memory device comprising a temperature detection circuit for tracking a temperature of the integrated memory device and producing an output signal on an output node and a control circuit coupled to the temperature detection circuit for receiving the output signal and adjusting an operation parameter of the integrated circuit memory device in response to the output signal, col. 1, lines 42-49).

Arimoto, Shiga and Chevallier are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a temperature detection circuit to determine a predetermined temperature because the output of the detection circuit my be used to adjust a memory operation, such as operating frequency (col. 6, lines 41-49), as taught by Chevallier.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al (US Patent No. 6,400,625), Shiga et al (US Patent No. 6,552,936) and Koh (US Patent No. 6,437,308).

For claim 10, the combined teachings of Arimoto and Shiga disclose the invention as per the rejection of claim 1 above.

These teachings fail to disclose the limitations of the current claim.

Koh, however, helps disclose a light detection circuit, wherein the read data control circuit performs control such that the microcomputer takes in the data read from the memory only when the light detection circuit detects light having a predetermined intensity (a light detection circuit employed in an electronic device, such as a portable transaction card, col. 1, lines 8-10; comparing a sensing circuit output with a reference voltage and generating an output, col. 2, lines 40-42).

Arimoto, Shiga and Koh are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a light detection circuit that detects light having a predetermined intensity in the presently claimed invention because this would allow for securing of information, and for operations for processing and storing information from the card to be inhibited (col. 1, lines 34-39), as taught by Koh.

### *Citation of Pertinent Prior Art*

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akagi (US Patent No. 6,434,096) discloses a temperature sensor detects the current apparatus temperature and triggers an operation after comparison of detected temperature to previous detections.

Matsuda (US PGPub No. 20020060659) discloses a trigger occurs in the reflected light detection circuit when reflected light of a predetermined intensity is detected by an apparatus for detecting light.

### *Conclusion*

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Contact Information***

12. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

6-19-06

PIERRE VITAL
PRIMARY EXAMINER